INNOLUX DISPLAY CORPORATION

LCD MODULE

APPLICATION NOTE

Customer:	**ALL**
LCD SIZE:	**7.0D**
Date:	**2009/3/9**
Version:	**H**

Remark
■ **With PCB**

Approved by	Reviewed by	Prepared by
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Record of Revision

Version	Revise Date	Page	Content
E	2008/3/18		The fifth version
F	2008/8/26		Add new production
G	2009/2/13		Reclassify and standardization
H	2009/3/9		Modify format

INNOLUX General

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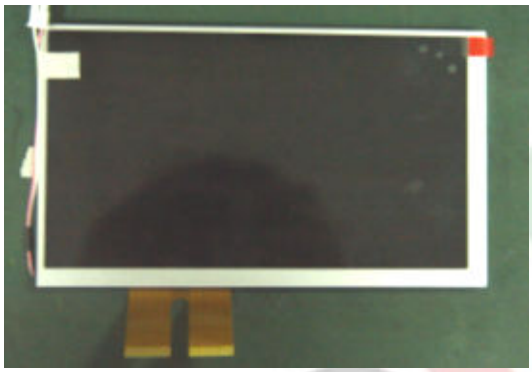
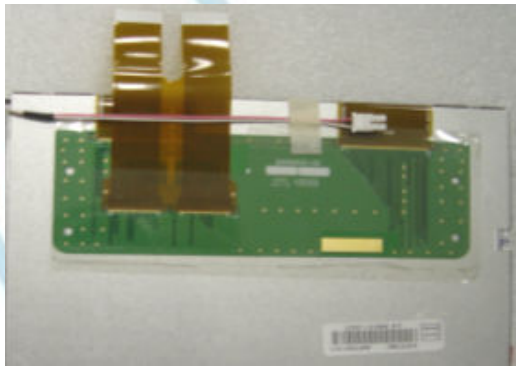
1. Module Introduction

1.1 Module Photo

Model	Module photo	
	Top side	Bottom side
AT070TN83V.3		
AT070TN82 AT070TN82V.1 AT070TN84V.1		

1.2 Module Comparison Table

Module name	T-con board input interface	Integrate LED driver	Pin Num.	Recommended connector
AT070TN82	TTL without T-con	NO	60 pin	AF 730L-A2G1T
AT070TN84 V.1	TTL without T-con	NO	60 pin	AF 730L-A2G1T
AT070TN83 V.3	TTL without T-con	NO	60 pin	AF 730L-A2G1T
AT070TN82 V.1	TTL without T-con	NO	60 pin	AF 730L-A2G1T

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2. Pin Assignment Table

Pin No.	Symbol	I/O	Function	Remark
1	POL	I	Polarity selection	
2	STVD	I/O	Vertical start pulse input when U/D= H	Note 1
3	OEV	I	Output enable	Note 4
4	CKV	I	Vertical clock	Note 5
5	STVU	I/O	Vertical start pulse input when U/D= L	Note 1
6	GND	P	Power Ground	
7	EDGSL	I	Select rising edge or falling edge	Note 6
8	DV_{DD}	P	Power for Digital Circuit	
9	V9	I	Gamma voltage level 9	
10	V_{GL}	P	Gate OFF voltage	
11	V2	I	Gamma voltage level 2	
12	V_{GH}	P	Gate ON voltage	
13	V6	I	Gamma voltage level 6	
14	U/D	I	Up/down selection	Note 1,2
15	V_{COM}	I	Common voltage	
16	GND	P	Power Ground	
17	AV_{DD}	P	Power Voltage for Analog Circuit	
18	V14	I	Gamma voltage level 14	
19	V11	I	Gamma voltage level 11	
20	V8	I	Gamma voltage level 8	
21	V5	I	Gamma voltage level 5	
22	V3	I	Gamma voltage level 3	
23	GND	P	Power Ground	
24	R5	I	Red data(MSB)	

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25	R4	I	Red data	
26	R3	I	Red data	
27	R2	I	Red data	
28	R1	I	Red data	
29	R0	I	Red data(LSB)	
30	GND	P	Power Ground	
31	GND	P	Power Ground	
32	G5	I	Green data(MSB)	
33	G4	I	Green data	
34	G3	I	Green data	
35	G2	I	Green data	
36	G1	I	Green data	
37	G0	I	Green data(LSB)	
38	STHL	I/O	Horizontal start pulse input when R/L = L	Note 1
39	REV	I	Control signal are inverted or not	Note 2
40	GND	I	Power Ground	
41	DCLK	I	Sample clock	
42	DV_{DD}	P	Power Voltage for Digital Circuit	
43	STHR	I/O	Horizontal start pulse input when R/L =H	Note 1
44	LD	I	Latches the polarity of outputs and Switches the new data to outputs	Note 3
45	B5	I	Blue data (MSB)	
46	B4	I	Blue data	
47	B3	I	Blue data	
48	B2	I	Blue data	
49	B1	I	Blue data	
50	B0	I	Blue data (LSB)	

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51	R/L	I	Right/ left selection	Note 1
52	V1	I	Gamma voltage level 1	
53	V4	I	Gamma voltage level 4	
54	V7	I	Gamma voltage level 7	
55	V10	I	Gamma voltage level 10	
56	V12	I	Gamma voltage level 12	
57	V13	I	Gamma voltage level 13	
58	AV_{DD}	P	Power for Analog Circuit	
59	GND	P	Power Ground	
60	V_{COM}	I	Common voltage	

I: input, O: output, P: Power

Note 1: Selection of scanning mode

Setting of scan control input		IN/OUT state for start pulse				Scanning direction
U/D	R/L	STVD	STVU	STHR	STHL	
GND	DV_{DD}	O	I	I	O	Up to down, left to right
DV_{DD}	GND	I	O	O	I	Down to up, right to left
GND	GND	O	I	O	I	Up to down, right to left
DV_{DD}	DV_{DD}	I	O	I	O	Down to up, left to right

Note 2: When REV="L", it's under normal operation.
When REV="H", these data will be inverted.
When use this function, it need your system T-con support.

Note 3: LD: latches the polarity of outputs and switches the new data to outputs.
At the rising edge latches the POL signal to control the polarity of outputs.
The pin also controls the switch of the line registers that switches the new data to output.
The LD may switch at any time even if the line data are not completely full

Note 4: OEV: Gate output enable.

Note 5: CKV: Gate output clock

Note 6: EDGSL: Choose raising edge or falling edge to match the timing characteristic.

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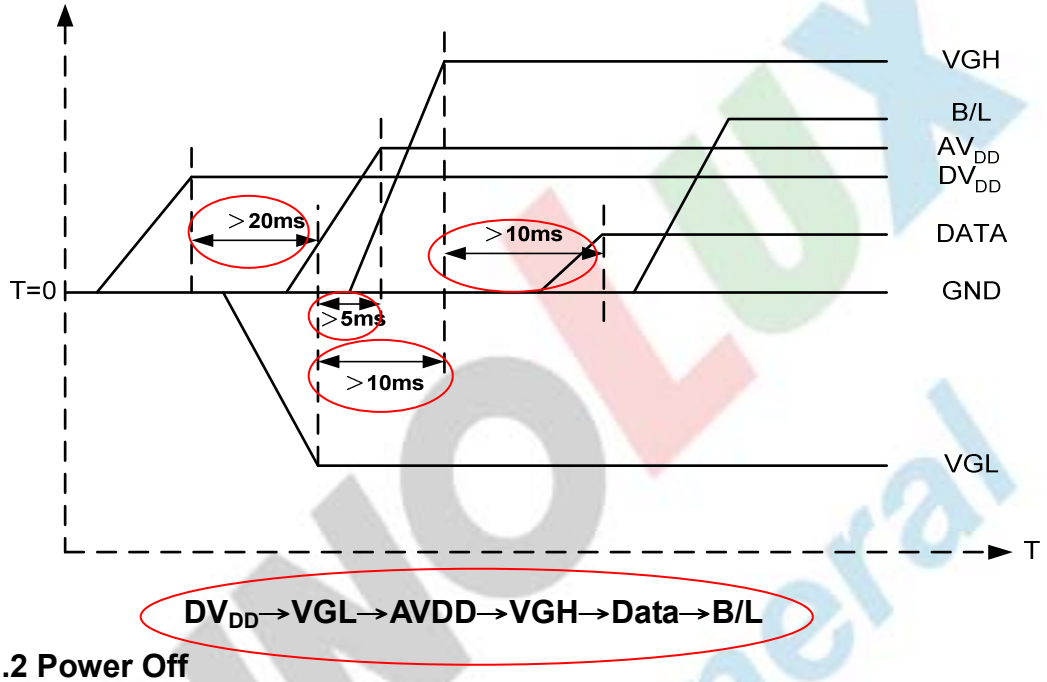
3. Power &Timing Characteristic

3.1. Power Sequence

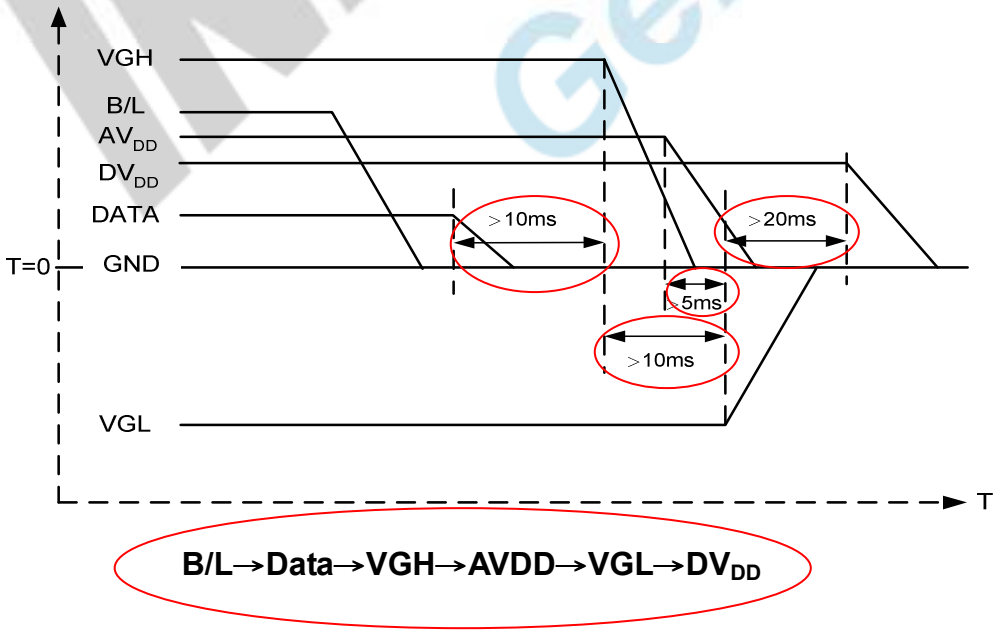
Customer should follow our product power sequence, other it would lead to display abnormal, please refer to the figures as below.

3.1.1 Power On



DV_{DD}→VGL→AVDD→VGH→Data→B/L

3.1.2 Power Off



B/L→Data→VGH→AVDD→VGL→DV_{DD}

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3.2 Power Operation Conditions

Customer should notice the red mark specially, if you do not follow it, it would lead to display abnormal.

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	DV_{DD}	3.0	3.3	3.6	V	Note 2
	AV_{DD}	10.2	10.4	10.6	V	
	V_{GH}	15.3	16.0	16.7	V	
	V_{GL}	-7.7	-7.0	-6.3	V	
Input signal voltage	V_{COM}	3.9	4.1	4.3	V	(V1+V14)/2= 5.2V
	V1~V7	0.4 AV_{DD}	-	AV_{DD} -0.1	V	
	V8~V14	0.1	-	0.6 AV_{DD}	V	
Input logic high voltage	V_{IH}	0.7 DV_{DD}	-	DV_{DD}	V	Note 3
Input logic low voltage	V_{IL}	0	-	0.3 DV_{DD}	V	

Note 1: Be sure to apply DV_{DD} and V_{GL} to the LCD first, and then apply V_{GH}.

Note 2: DV_{DD} setting should match the signals output voltage (refer to Note 3) of customer's system board.

Note 3: POL, STVD, OEV, CKV, STVU, EDGSL, U/D, STHL, REV, DCLK, STHR, LD, R/L. R0~R5, G0~G5, B0~B5.

3.3 Timing Description

Input signals must follow our timing specification, Otherwise the LCM will display abnormally.
About the detail timing parameters of LCD display, please follow the product specification

3.3.1. Timing Diagram

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DCLK frequency	Fdclk	-	40	45	MHz	
DCLK cycle	Tcph	22	25	-	ns	

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DCLK pulse width	Tcw	8	-	-	ns	
Data set-up time	Tsu	4	-	-	ns	
Data hold time	Thd	2	-	-	ns	
Time that the last data to LD	Tld	1	-	-	Tcph	
Pulse width of LD	Twld	2	-	-	Tcph	
Time that LD to STHL/R	Tlds	5	-	-	Tcph	
POL set-up time	Tpsu	6	-	-	ns	
POL hold time	Tphd	6	-	-	ns	
CKV frequency	Fvclk	-	-	200	KHz	
CKV rise time	Trck	-	-	100	ns	
CKV falling time	Tfck	-	-	100	ns	
CKV pulse width	PWCLK	500	-	-	ns	
Horizontal display timing range	Tdh	-	800	-	Tcph	
Horizontal timing range	Th	-	1056	-	Tcph	
STVU/D setup time	Tsuv	200	-	-	ns	
STVU/D hold time	Thdv	300	-	-	ns	
STVU/D delay time	Tdt	-	-	500	ns	
Driver output delay time	Tdo	-	-	900	ns	
Output rise time	Ttlh	-	500	1000	ns	
Output falling time	Tthl	-	400	800	ns	
OEV pulse width	Twcl	1	-	-	us	
OEV to Driver output delay time	Toe	-	-	900	ns	
Horizontal lines per field	Tv	512	525	610	Tdh	
Vertical display timing range	Tvd	-	480	-	Tdh	

4. Software Introduction

NA

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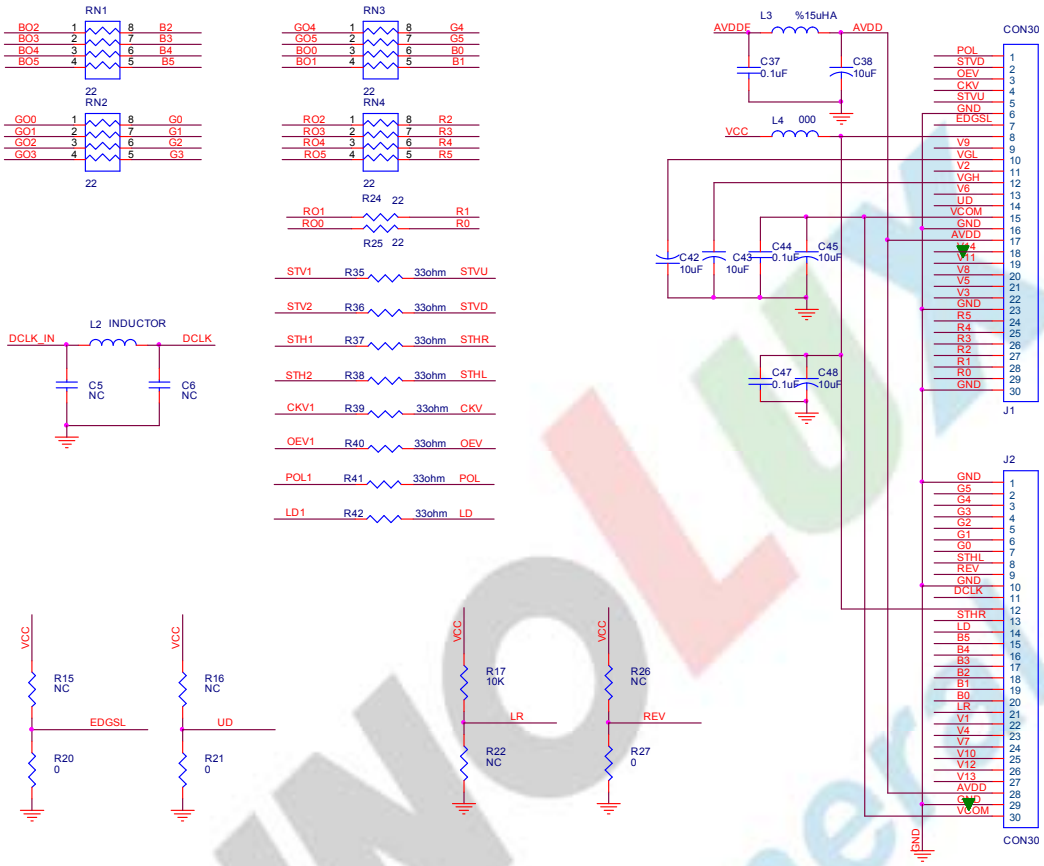
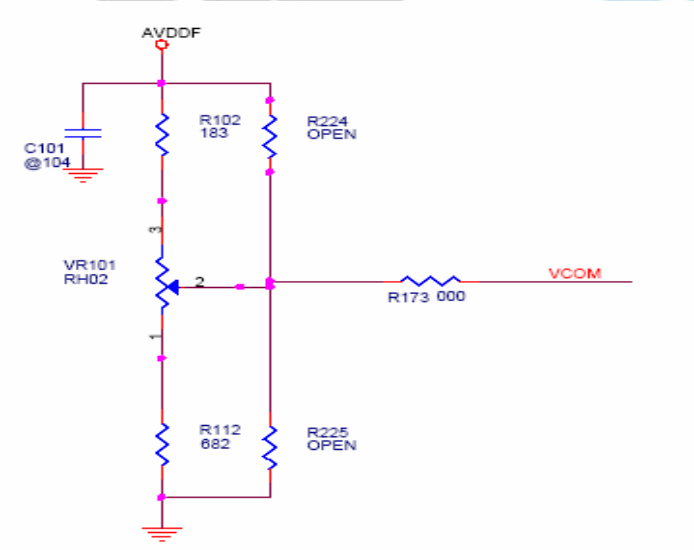
5. Reference Circuit

5.1 Interface reference circuit



5.2 Vcom Reference Circuit



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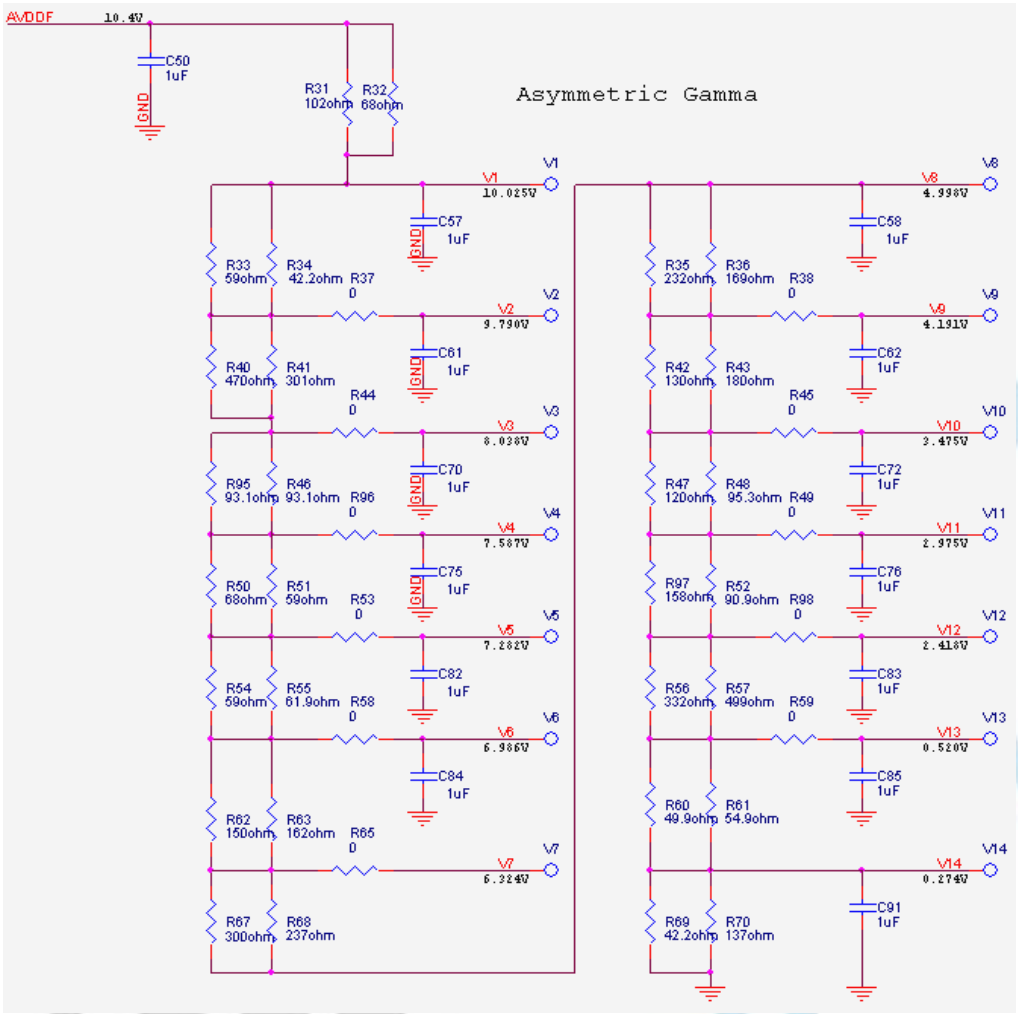
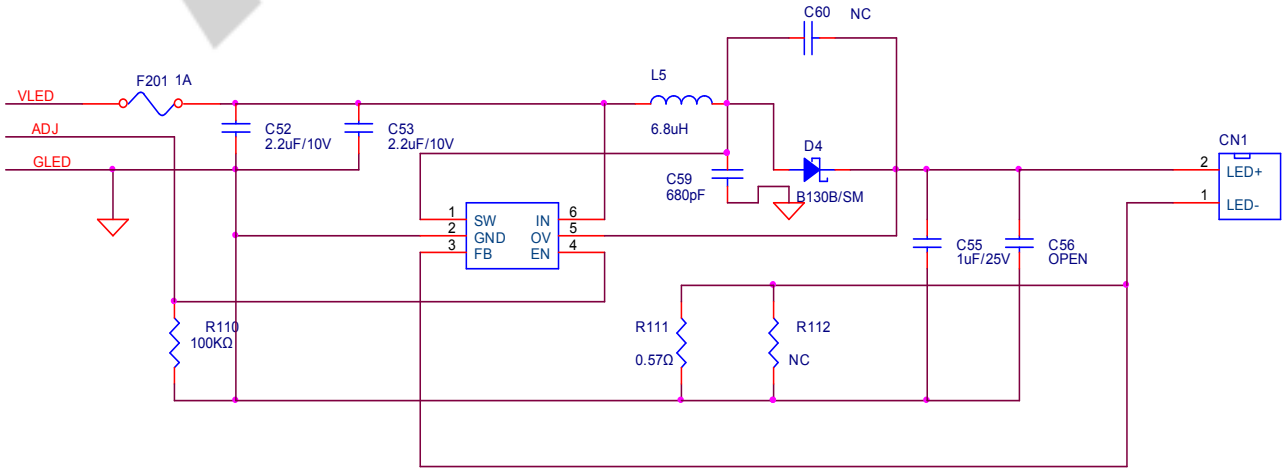
5.3Gamma Reference Circuit



AVDD	V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14
10.4	10.03	9.79	8.04	7.59	7.28	6.99	6.32	5.1	4.19	3.47	2.97	2.42	0.52	0.27

5.4 Backlight Driver Reference Circuit



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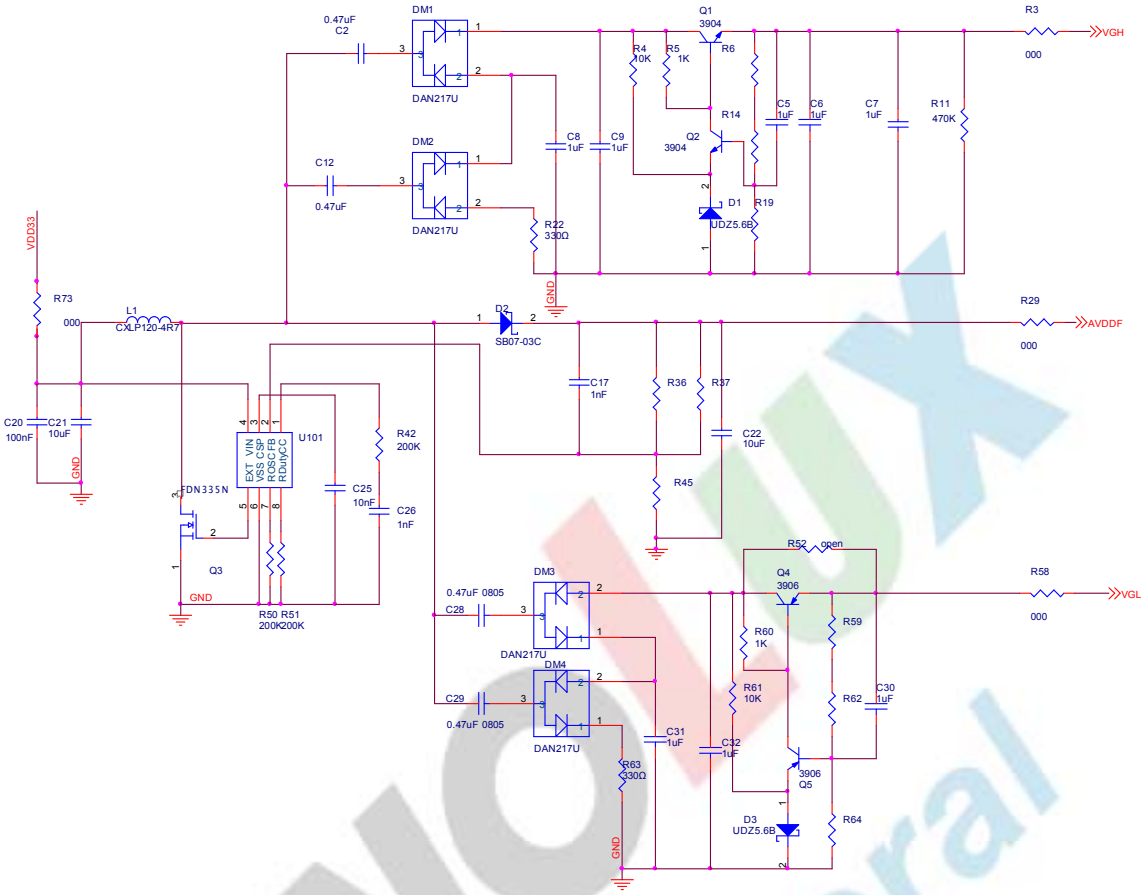
5.5 DC/DC Reference Circuit



5.6 Vendor Recommend

ITEM	VENDER	TYPE	Remark
DC-DC	Fiti power	FP6791	
LED driver	Fiti power	FP6796	
	MPS	MP3202	Suggestion PWM Frequency 100-300Hz
		MP3302	Suggestion PWM Frequency 100-300Hz or 1k-20kHz
T-con(TTL)	Fiti power	EK6709	
	Novatek	NT30703	

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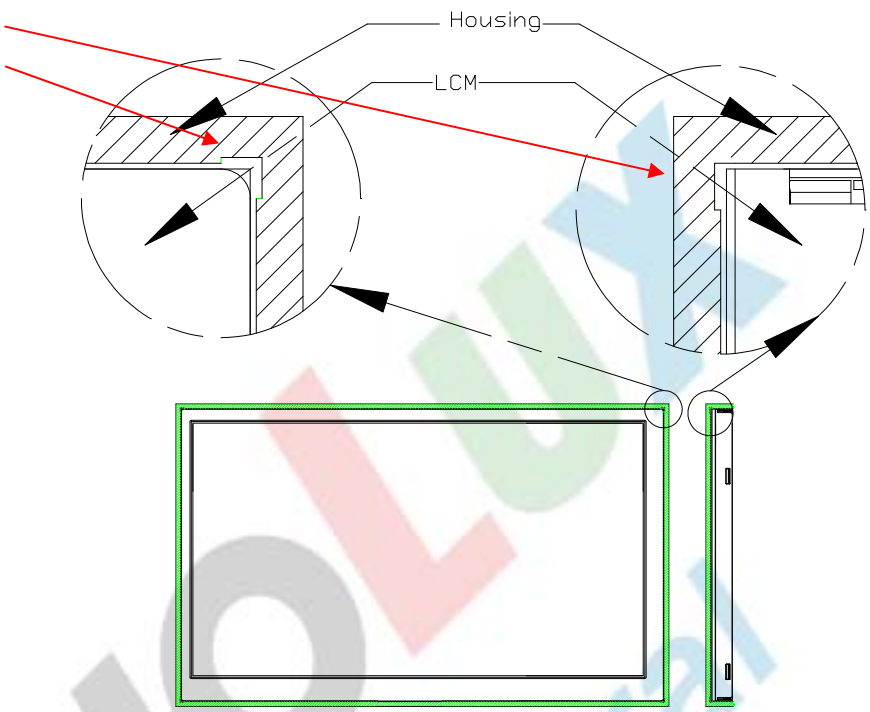
6.Suggestions for housing design.

6.1 LCM corner /edge avoidable cutting.

If you design a avoidable cutting as the right drawing. LCM will easier to assemble in the housing.
When you use the LCM with TSP, the cutting will avoid damage the edge or corner of TSP during the assembly.



Suggestions of housing design

6.2 Housing opening design guide.

6.2.1 With TSP

Because touch film is made of flexible PET, any unexpected touch with it would cause malfunction of touch panel. So here a sponge between touch panel and plastic housing is recommended for users. And the drawing will show you how to design the housing and sponge.

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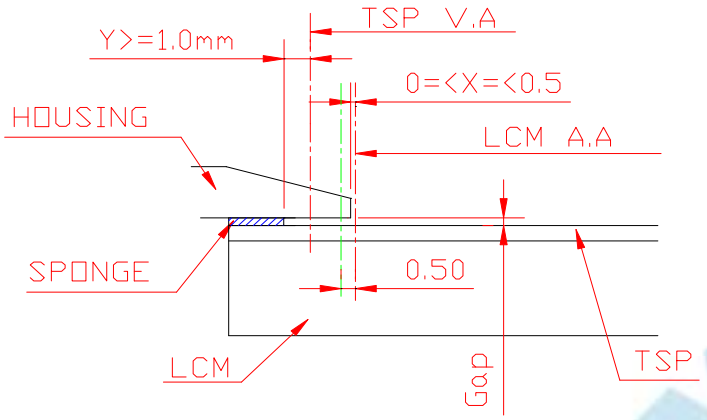
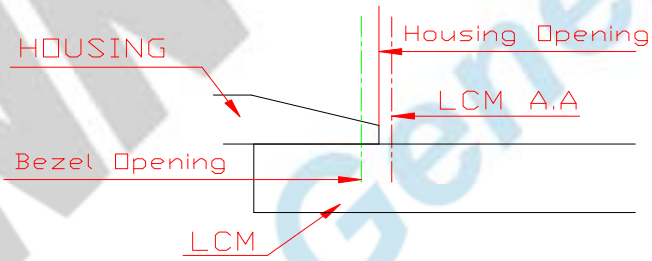


Section sketch (with TSP)

Notes: 1. X is the distance from LCM A.A to housing opening.
2. Y is the distance from TSP V.A to Sponge opening.
3. The active force will be bigger when you touch the area near the housing opening.
4. If you want to provide more protection for LCM, you can add same buffer material on the bottom of LCM.

6.2.2 Without TSP



Section sketch(without TSP)

Notes: 1. Housing opening mast bigger than LCMA.A and cover the bezel .
2. If you want to provide more protection for LCM, you can add same buffer material on the top or bottom of LCM.

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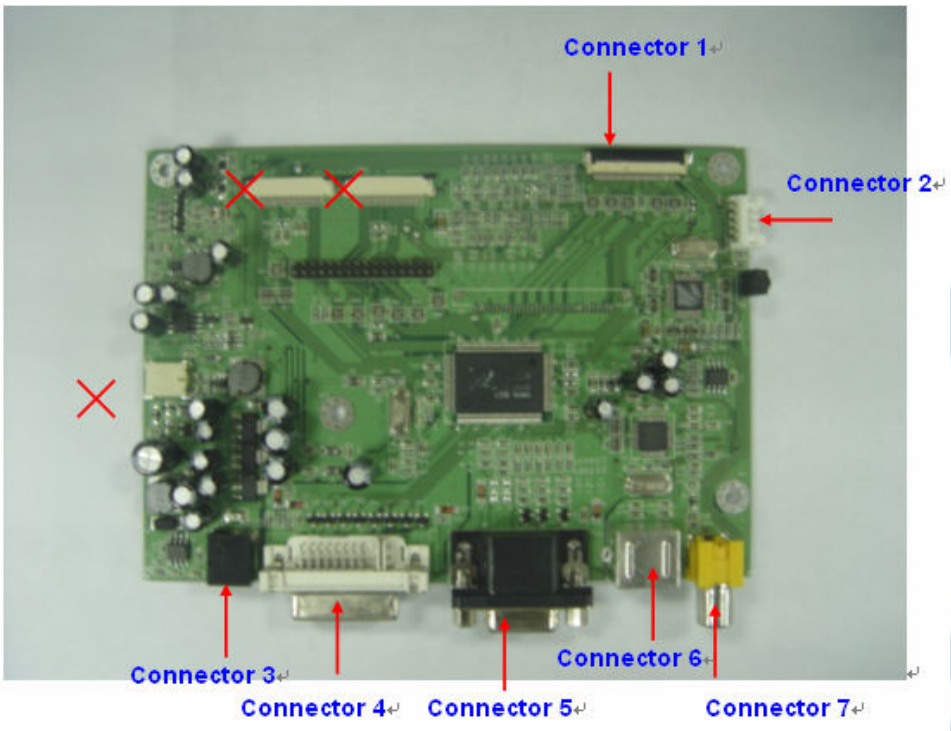
7.Demo Board Introduce

7.1 Interface of Demo Board



Connector	I/O	Function
1	O	connector
2	I	The hand-off controller of CVBS and D-Sub
3	P	12V DC input
4	I	DVI signal input
5	I	VGA signal input
6	I	S-video
7	I	CVBS

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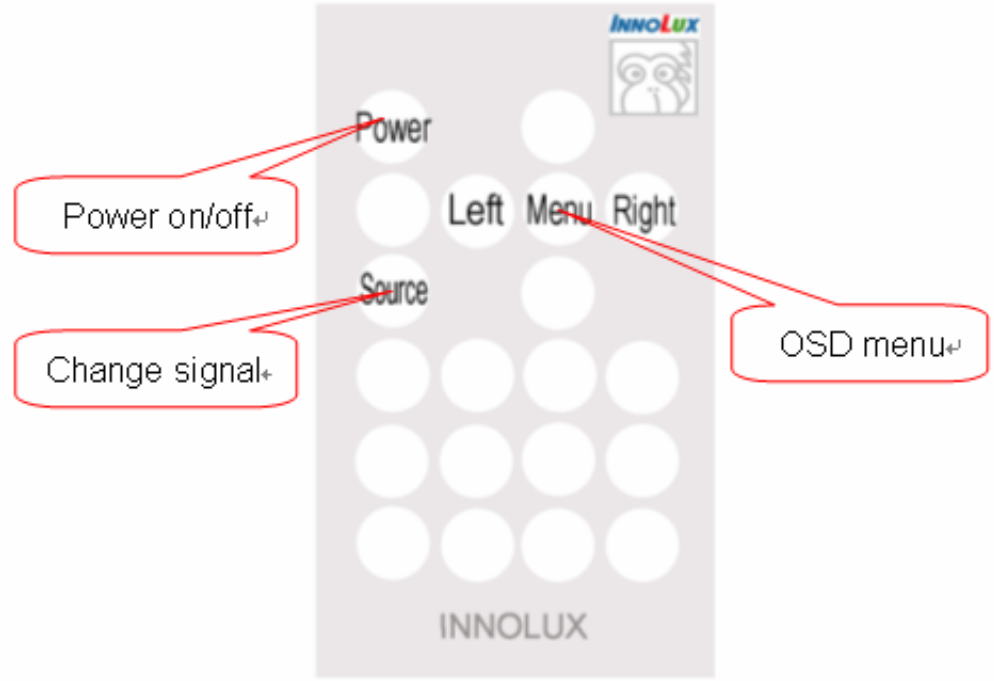
7.2 Interface of Remote control



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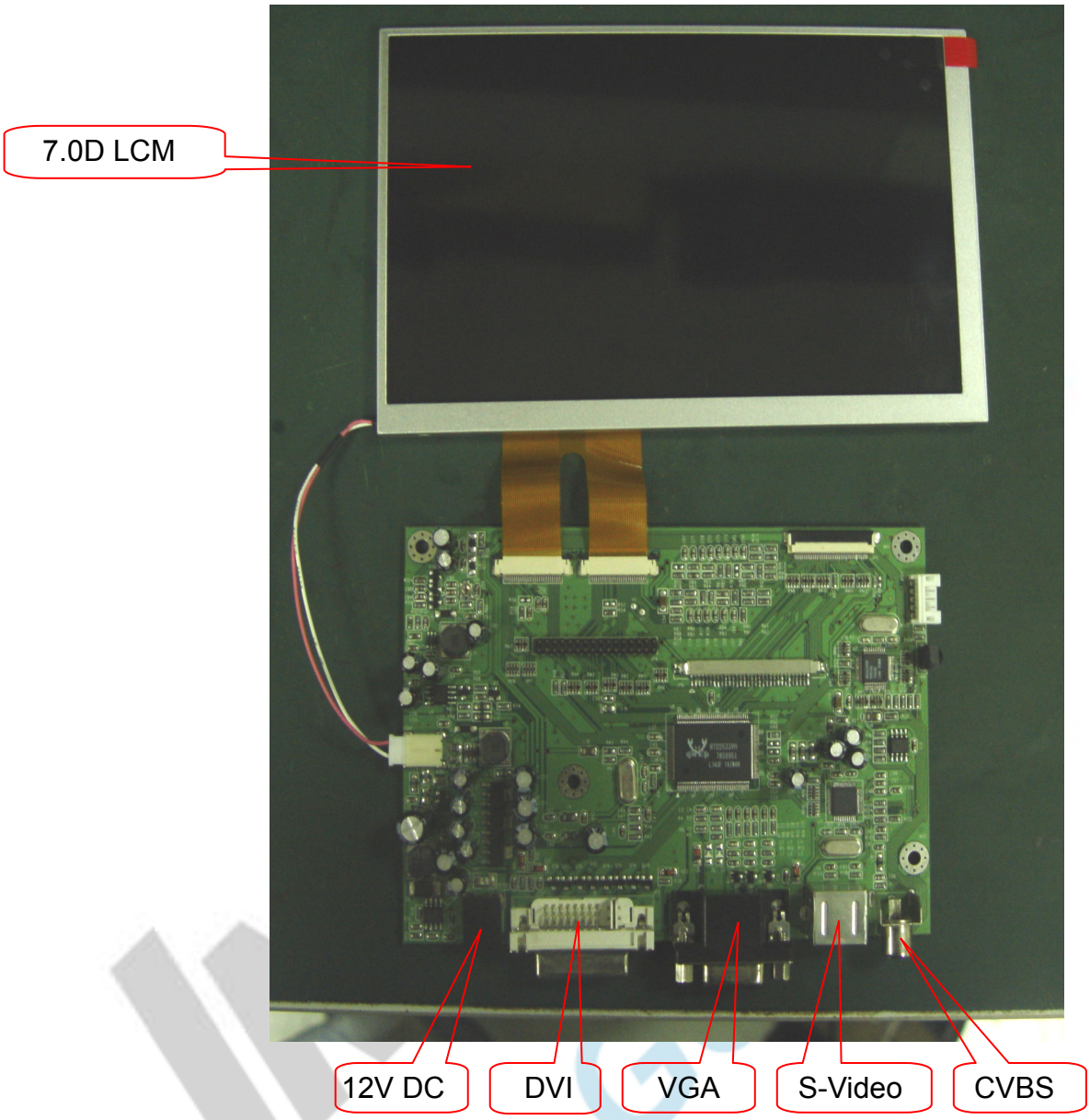
7.3 Linking LCM



Notes:

1. We don't guarantee any power & timing & optical characteristic measured by INL control board.
2. INL control board is just for demo INL digital panel.

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